CLEAN VERSION OF CLAIM PAGES 15 - 24

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WHAT IS CLAIMED

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1. A method of manufacturing an interconnect for a magnetoresistive memory on a semiconductor substrate comprising:

(a) forming an initial dielectric layer overlying the semiconductor substrate;

(b) planarizing the initial dielectric layer;

(c) forming a magnetoresistive storage layer overlying the initial dielectric layer;

(d) forming an electrically-conductive initial stop layer overlying the magnetoresistive storage layer;

(e) forming an electrically-conductive final stop layer overlying the initial stop layer;

(f) forming a hardmask layer overlying the final stop layer;

(g) etching the hardmask layer and the final stop layer until the initial stop layer is exposed to define an etch region;

(h) etching through the initial stop layer and the magnetoresistive storage layer until the initial dielectric layer is exposed using the etch region as an etch opening;

(i) forming an isolation layer extending over the hardmask layer and into the etch region, the isolation layer having sufficient thickness to fill in the gaps created by etching the etch region;

(j) planarizing the isolation layer until regions of the final stop layer are exposed; and

(k) forming an interconnect layer over the exposed regions of the final stop layer.

2. The method of claim 1 wherein forming the initial dielectric layer comprises forming a layer of silicon nitride.

3. The method of claim 1 wherein planarizing the initial dielectric layer is completed using a chemical mechanical polish.

4. The method of claim 1 wherein forming the magnetoresistive storage layer comprises forming a plurality of layers selected from the group consisting of cobalt, copper, nickel, iron, tantalum, and combinations thereof.

5. The method of claim 1 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is greater than the etch selectivity of the hardmask layer.

6. The method of claim 5 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is 25 times greater than the etch selectivity of the hardmask layer.

7. The method of claim 1 wherein forming the initial stop layer comprises forming a layer consisting of chromium and silicon.

8. The method of claim 1 wherein forming the final stop layer comprises forming a layer which has a chemical mechanical polish stop selectivity which is greater than the hardmask layer.

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9. The method of claim 1 wherein forming the final stop layer comprises forming a layer consisting of titanium and tungsten.

10. The method of claim 1 wherein forming the hardmask layer comprises forming a layer consisting of silicon dioxide.

11. The method of claim 1 wherein etching through the initial stop layer and the magnetoresistive storage layer is completed using blanket ion milling.

12. The method of claim 1 wherein etching the hardmask layer and the final stop layer until the initial stop layer is exposed is completed using a dry etch.

13. The method of claim 1 wherein forming the isolation layer comprises:

forming an barrier layer extending over the hardmask layer and into the etch region to conformally overlie the hardmask layer and the exposed portions of the final stop layer, the initial stop layer, the magnetoresistive storage layer and the initial dielectric layer in the etch region; and

forming a final dielectric layer over the barrier layer wherein the final dielectric layer has sufficient thickness to fill in the gaps created by etching the etch region.

14. The method of claim 1 wherein forming the barrier layer comprises forming a layer consisting of silicon nitride.

15. The method of claim 1 wherein planarizing the isolation layer is completed using a chemical mechanical polish.

16. The method of claim 1 wherein forming the interconnect layer comprises forming a layer consisting of titanium and tungsten.

17. A method of manufacturing an interconnect for a magnetoresistive memory array comprising:

(a) providing a semiconductor substrate;

(b) forming an initial dielectric layer overlying the semiconductor substrate;

(c) planarizing the initial dielectric layer;

(d) forming a magnetoresistive storage layer overlying the initial dielectric layer;

(e) forming an electrically-conductive initial stop layer overlying the magnetoresistive storage layer;

(f) forming an electrically-conductive final stop layer overlying the initial stop layer;

(g) forming a hardmask layer overlying the final stop layer;

(h) etching portions of the hardmask layer and the final stop layer until the initial stop layer is exposed to define a plurality of etch regions;

(i) forming a plurality of magnetoresistive memory storage bits by etching through the initial stop layer and the magnetoresistive storage layer until the initial dielectric layer is exposed using the plurality of etch regions as etch openings;

(j) forming an isolation layer extending over the hardmask layer and into the plurality of etch regions, the isolation layer having sufficient thickness to fill in the gaps created by etching the plurality of etch regions;

(k) planarizing the isolation layer until a plurality of regions of the final stop layer are exposed; and

(l) forming a plurality of interconnects over portions of the plurality of regions of the final stop layer to interconnect each one of the plurality of magnetoresistive memory storage bits to another one of the plurality of magnetoresistive memory storage bits.

18. The method of claim 17 wherein forming the initial dielectric layer comprises forming a layer of silicon nitride.

19. The method of claim 17 wherein planarizing the initial dielectric layer is completed using a chemical mechanical polish.

20. The method of claim 17 wherein forming the magnetoresistive storage layer comprises forming a plurality of layers selected from the group consisting of cobalt, copper, nickel, iron, tantalum, and combinations thereof.

21. The method of claim 17 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is greater than the etch selectivity of the hardmask layer.

22. The method of claim 21 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is 25 times greater than the etch selectivity of the hardmask layer.

23. The method of claim 17 wherein forming the initial stop layer comprises forming a layer consisting of chromium and silicon.

24. The method of claim 17 wherein forming the final stop layer comprises forming a layer which has a chemical mechanical polish stop selectivity which is greater than the hardmask layer.

25. The method of claim 17 wherein forming the final stop layer comprises forming a layer consisting of titanium and tungsten.

26. The method of claim 17 wherein forming the hardmask layer comprises forming a layer consisting of silicon dioxide.

27. The method of claim 17 wherein patterning a plurality of magnetoresistive memory storage bits by etching through the initial stop layer and the magnetoresistive storage layer is completed using blanket ion milling.

28. The method of claim 17 wherein etching the hardmask layer and the final stop layer until the initial stop layer is exposed is completed using a dry etch.

29. The method of claim 17 wherein forming the isolation layer comprises:

forming a barrier layer extending over the hardmask layer and into the plurality of etch regions to conformally overlie the hardmask layer and the exposed portions of the final stop layer, the initial stop layer, the magnetoresistive storage layer and the initial dielectric layer in the plurality of etch regions; and

forming a final dielectric layer over the barrier layer wherein the final dielectric layer has sufficient thickness to fill in the gaps created by etching the plurality of etch regions.

30. The method of claim 29 wherein forming the barrier layer comprises forming a layer consisting of silicon nitride.

31. The method of claim 17 wherein planarizing the isolation layer is completed using a chemical mechanical polish.

32. The method of claim 17 wherein forming a plurality of interconnects over portions of the plurality of regions of the final stop layer comprises:

depositing a layer of interconnect metal which overlies the plurality of regions of the final stop layer; and

selectively etching the layer of interconnect metal to interconnect each one of the plurality of magnetoresistive memory storage bits to another one of the plurality of magnetoresistive memory storage bits.

33. The method of claim 32 wherein depositing a layer of interconnect metal comprises depositing a layer consisting of titanium and tungsten.

34. The method of claim 17 wherein providing a semiconductor substrate further comprises forming an initial layer of metal overlying the semiconductor substrate, the initial dielectric layer overlying the initial layer of metal.

35. A method of manufacturing an interconnect for a magnetoresistive memory storage device having a plurality of magnetoresistive memory storage bits and read and write control circuitry for reading data from and writing data to the plurality of magnetoresistive memory storage bits, comprising:

(a) providing a semiconductor substrate;

(b) forming the read and write control circuitry on the semiconductor substrate;

(c) forming an initial dielectric layer overlying the read and write control circuitry;

(d) planarizing the initial dielectric layer;

(e) forming a magnetoresistive storage layer overlying the initial dielectric layer;

(f) forming an electrically-conductive initial stop layer overlying the magnetoresistive storage layer;

(g) forming an electrically-conductive final stop layer overlying the initial stop layer;

(h) forming a hardmask layer overlying the final stop layer;

(i) etching portions of the hardmask layer and the final stop layer until the initial stop layer is exposed to define a plurality of etch regions;

(j) forming the plurality of magnetoresistive memory storage bits by etching through the initial stop layer and the magnetoresistive storage layer until the initial dielectric layer is exposed using the plurality of etch regions as etch openings;

(k) forming an isolation layer extending over the hardmask layer and into the plurality of etch regions, the isolation layer having sufficient thickness to fill in the gaps created by etching the plurality of etch regions;

(l) planarizing the isolation layer until a plurality of regions of the final stop layer are exposed; and

(m) forming a plurality of interconnects over portions of the plurality of regions of the final stop layer to interconnect each one of the plurality of magnetoresistive memory storage bits to another one of the plurality of magnetoresistive memory storage bits.

36. The method of claim 35 wherein forming the initial dielectric layer comprises forming a layer of silicon nitride.

37. The method of claim 35 wherein planarizing the initial dielectric layer is completed using a chemical mechanical polish.

38. The method of claim 35 wherein forming the magnetoresistive storage layer comprises forming a plurality of layers selected from the group consisting of cobalt, copper, nickel, iron, tantalum, and combinations thereof.

39. The method of claim 35 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is greater than the etch selectivity of the hardmask layer.

40. The method of claim 39 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is 25 times greater than the etch selectivity of the hardmask layer.

41. The method of claim 35 wherein forming the initial stop layer comprises forming a layer consisting of chromium and silicon.

42. The method of claim 35 wherein forming the final stop layer comprises forming a layer which has a chemical mechanical polish stop selectivity which is greater than the hardmask layer.

43. The method of claim 35 wherein forming the final stop layer comprises forming a layer consisting of titanium and tungsten.

44. The method of claim 35 wherein forming the hardmask layer comprises forming a layer consisting of silicon dioxide.

45. The method of claim 35 wherein patterning a plurality of magnetoresistive memory storage bits by etching through the initial stop layer and the magnetoresistive storage layer is completed using blanket ion milling.

46. The method of claim 35 wherein etching the hardmask layer and the final stop layer until the initial stop layer is exposed is completed using a dry etch.

47. The method of claim 35 wherein forming the isolation layer comprises:

forming a barrier layer extending over the hardmask layer and into the plurality of etch regions to conformally overlie the hardmask layer and the exposed portions of the final stop layer, the initial stop layer, the magnetoresistive storage layer and the initial dielectric layer in the plurality of etch regions; and

forming a final dielectric layer over the barrier layer wherein the final dielectric layer has sufficient thickness to fill in the gaps created by etching the plurality of etch regions.

48. The method of claim 47 wherein forming the barrier layer comprises forming a layer consisting of silicon nitride.

49. The method of claim 35 wherein planarizing the isolation layer is completed using a chemical mechanical polish.

50. The method of claim 35 wherein forming a plurality of interconnects over portions of the plurality of regions of the final stop layer comprises:

depositing a layer of interconnect metal which overlies the plurality of regions of the final stop layer; and

selectively etching the layer of interconnect metal to interconnect each one of the plurality of magnetoresistive memory storage bits to another one of the plurality of magnetoresistive memory storage bits.

51. The method of claim 50 wherein depositing a layer of interconnect metal comprises depositing a layer consisting of titanium and tungsten.

52. The method of claim 35 wherein forming the read and write control circuitry on the semiconductor substrate comprises using a complementary metal-oxide semiconductor process.

53. The method of claim 35 wherein providing a semiconductor substrate further comprises forming an initial layer of metal overlying the semiconductor substrate, the initial dielectric layer overlying the initial layer of metal.

54. A method of manufacturing an interconnect for a magnetoresistive memory on a semiconductor substrate comprising:

(a) forming an initial dielectric layer overlying the semiconductor substrate;

(b) planarizing the initial dielectric layer;

(c) forming a magnetoresistive storage layer overlying the initial dielectric layer;

(d) forming an electrically-conductive stop layer overlying the magnetoresistive storage layer;

(e) forming a hardmask layer overlying the stop layer;

(f) etching the hardmask layer until the stop layer is exposed to define an etch region;

(g) etching through the stop layer and the magnetoresistive storage layer until the initial dielectric layer is exposed using the etch region as an etch opening;

(h) forming an isolation layer extending over the hardmask layer and into the etch region, the isolation layer having sufficient thickness to fill in the gaps created by etching the etch region;

(i) planarizing the isolation layer until regions of the stop layer are exposed; and

(j) forming an interconnect layer over the exposed regions of the stop layer.

55. The method of claim 54, further comprising:

forming a second electrically-conductive stop layer over the stop layer; and

wherein etching through the hardmask layer includes etching through the second stop layer.

56. A method of manufacturing an interconnect for a magnetoresistive memory on a semiconductor substrate comprising:

(a) forming an initial dielectric layer overlying the semiconductor substrate;

(b) planarizing the initial dielectric layer;

(c) forming a magnetoresistive storage layer overlying the initial dielectric layer;

(d) forming an electrically conductive stop layer overlying the magnetoresistive storage layer;

(e) forming a hardmask layer overlying the stop layer, the hardmask layer having an etch selectivity less than the etch selectivity of the stop layer;

(f) etching the hardmask layer until the stop layer is exposed to define an etch region;

(g) etching through the stop layer and the magnetoresistive storage layer using blanket ion milling until the initial dielectric layer is exposed using the etch region as an etch opening;

(h) forming an isolation layer extending over the hardmask layer and into the etch region, the isolation layer having sufficient thickness to fill in the gaps created by etching the etch region;

(i) planarizing the isolation layer using chemical mechanical polishing until regions of the stop layer are exposed; and

(j) forming an interconnect layer over the exposed regions of the stop layer.

57. The method of claim 56, further comprising:

forming a second electrically conductive stop layer over the stop layer; and

wherein etching through the hardmask layer includes etching through the second stop layer.

58. The method of claim 57 wherein forming the second stop layer comprises forming a layer which has a chemical mechanical polish stop selectivity which is greater than the hardmask layer.

59. A method of forming a high current, electromigration-resistant metal interconnect between circuit elements on a semiconductor substrate, comprising:

(a) forming a non-conducting layer over the semiconductor substrate;

(b) planarizing the non-conducting layer;

(c) forming a circuit element layer over the non-conducting layer;

(d) forming an electrically-conducting stop layer over the circuit element layer;

(e) forming a hardmask layer over the stop layer;

(f) etching the hardmask layer to expose the stop layer to define an etch region;

(g) etching through the stop layer and the circuit element layer until the non-conducting layer is exposed using the etch region as an etch opening;

(h) forming an isolation layer extending over the hardmask layer and into the etch region, the isolation layer having sufficient thickness to fill in the gaps created by etching the etch region;

(i) planarizing the isolation layer until regions of the stop layer are exposed; and

(j) forming an interconnect layer over the exposed regions of the stop layer.

60. The method of claim 59, further comprising:

forming a second electrically conductive stop layer over the stop layer; and

wherein etching through the hardmask layer includes etching through the second stop layer.

61. The method of claim 60 wherein forming the second stop layer comprises forming a layer which has a chemical mechanical polish stop selectivity which is greater than the hardmask layer.

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